A Robust High Voltage Si LDMOS Model Extraction Process to Achieve First Pass Linear RFIC Amplifier Design Success

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Abstract — **A robust model extraction procedure was developed for a high voltage Si LDMOS RFIC process to achieve first pass linear RFIC amplifier design success. The model extraction process utilizes pulsed isothermal small-signal S-parameter measurements and extracted large-signal Root Models at three different temperatures to extract model parameters for Motorola's Electro-Thermal (MET) FET analytical model. Large-signal model validation was performed against loadpull measurements under 1-tone and 2-tone stimuli. Also, the models were developed into a design kit within Agilent® EEsof®'s ADS® (Advanced Design System) to design a wide-band 30 Watt power amplifier IC which achieved first pass design success.**

I. INTRODUCTION

The design of highly linear power amplifiers for use in wireless infrastructure systems continues to challenge designers as well as tax the utmost performance from existing high-power high-voltage Si LDMOS transistors. A clear trend in this industry is to increase the linear power density and to increase the level of integration. Therefore, for first pass RFIC linear amplifier design success, a robust model extraction procedure must be developed to accurately predict its nonlinear electrical performance.

To this end, isothermal small-signal models were first extracted to accurately determine the parasitic resistances and inductances. The small-signal models were developed with the use of pulsed S-parameter data [1]. Once the parasitic resistances and inductances are known, the large-signal model extraction process can be initiated.

Two different nonlinear transistor models were provided to designers, an isothermal Root model [2,3] and an MET LDMOS electro-thermal model [4]. Both nonlinear models were validated against loadpull measurements.

Models were also developed for all the passive components used in the design of the power amplifier circuits on the high-voltage Si LDMOS RFIC technology. All models were implemented into a design kit in ADS, with both electrical and artwork descriptions. The end result was the implementation of a robust design environment that is scalable, versatile and easy to use.

Examples of the measured versus simulated response of a 30-Watt power amplifier IC will be shown, demonstrating the accuracy of the high power transistor and passive component models.

II. SMALL-SIGNAL MODEL EXTRACTION PROCESS

In order to accurately extract large-signal FET models, the parasitic resistances and inductances must first be extracted. This is often done by performing cold and hot FET S-parameter measurements and by performing a direct extraction of the parasitic elements from the fixture de-embedded Z-parameters at frequencies above 12 GHz.

Pulsed S-parameter measurements were made for several devices of different gate periphery at multiple quiescent drain current points and to a drain-to-source voltage of 26 Volts. A pulsed DC and S-parameter measurement system was used to decouple the electrical and thermal behavior of the devices. In order to ensure consistency devices were taken from the same wafer and had identical gate lengths and gate widths; the only difference between devices was the number of gate fingers.

All of the measured S-parameters were de-embedded to the intrinsic device reference plane and a direct extraction of the FET equivalent circuit parameters was performed. These intrinsic model parameters along with the parasitic resistances and inductances provided an initial starting point for a global optimization procedure over bias and over gate peripheries.

The first pass of the global optimization process is performed on a given device size at multiple current density bias points, which were typically 0, 2, 3, 4, 4.5, 6, 12 mA per mm and typical drain-to-source voltage. The FET extrinsic and intrinsic parameters were allowed to vary and all bias conditions were optimized simultaneously. However, the FET's parasitic resistances and inductances were kept the same for each bias. This assures that the global optimization results in a unique set of parasitic resistances and inductances for a given transistor size.

The second pass of the global optimization process is performed over a range of device sizes at the same drain

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current density. However, at this stage, the parasitic resistance and inductance values are held constant while a unique set of intrinsic model parameters, normalized per millimeter of gate periphery, are allowed to vary.

The results of this two step global optimization process is a unique set of parasitic resistances and inductances, which are bias independent for each device size, and a unique set of normalized intrinsic model parameters at each bias point. The accurate extraction of the parasitic elements is essential to begin the large-signal model extraction.

III. LARGE-SIGNAL MODEL EXTRACTION

Motorola provides two types of large-signal models to its RFIC designers, the measurement table-based Root model and the analytical equation based MET (Motorola's Electro-Thermal) model. Both models have their advantages and disadvantages. The Root model provides good simulation results compared to measured data and it is easy to extract using Agilent's ICCAP® software. One of the main disadvantages is that it must extrapolate to simulate data outside of its measured domain, which might mean simulating at a different frequency, or bias point where it was not extracted. Another disadvantage is the inability to link electrical and thermal behavior.

The MET model is an electro-thermal equation based model, which uses a thermal RC subcircuit to link the electrical and thermal behavior of the device. One of the main disadvantages of the MET model is that it is difficult to extract. First, several pulsed DC IV and pulsed S-parameters measurements must be performed at different temperatures, insuring an isothermal characterization environment. The MET model parameters that describe the drain current behavior are obtained by performing a global optimization over bias and temperature of all the pulsed DC IV data. From the pulsed S-parameter data, the CV (capacitance vs. voltage) behavior can be obtained by means of fitting small-signal models over bias at each temperature. Then the MET model parameters that describe the CV behavior can finally be obtained. This extraction procedure is inefficient and quite time-consuming.

Since extracting the Root model was quite easy once the parasitics are known, a procedure was developed to extract the MET model from Root model simulated data. This eliminates the time spent in the lab making several pulsed measurements to extract the MET model parameters. Instead, isothermal Root models were extracted at three different temperatures, 25°, 75°, and 125° C. With these models, the simulator can be used to generate all the data required to extract the MET model parameters, namely DC-IV and CV over temperature.

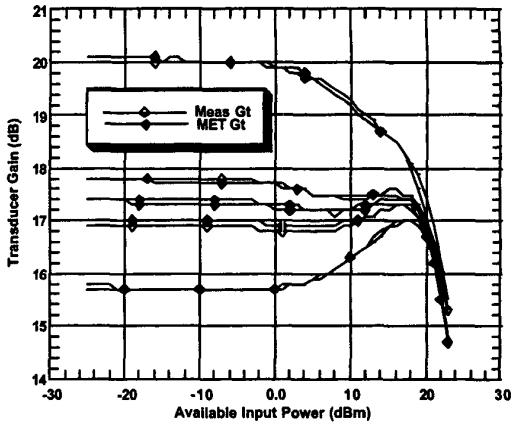

Fig. 1 Measured and simulated MET model transducer gain vs. available input power for a 10.2 mm LDMOS FET.

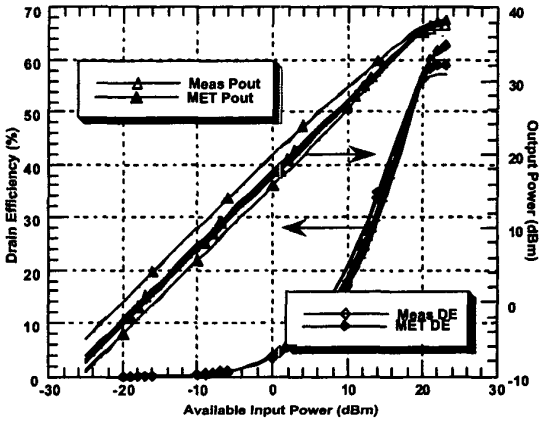

Fig. 2. Measured and simulated MET model drain efficiency and Pout vs. available input power for a 10.2 mm LDMOS FET.

IV. VALIDATION OF NON-LINEAR MODELS

Before distributing the extracted Root and MET models to the RFIC designers, the models must first be validated. The validation process involves measuring loadpull data under 1-tone and 2-tone stimuli on the same device that was used to extract the Root and MET models. In this case, the device has 10.2 mm of gate periphery. The devices were measured with an automated Maury[7] loadpull station. The source and load impedances were chosen for best input return loss and a trade-off in power-added efficiency and output power. Then the input power was swept from essentially small-signal to 3 dB into compression at which time gain, output power, efficiency,

and intermodulation distortion (2-tone only) was measured. All loadpull measurements were performed at 2.14 GHz. The two-tone loadpull measurements were performed with a tone separation of 100 KHz. All measurements were performed in a fixtured environment with a drain-to-source voltage of 26 V, at several quiescent bias points yielding drain-to-source current densities ranging from 2 to 12 mA per mm of gate periphery.

Figs. 1 through 6 illustrate measured loadpull data versus simulated model data under 1-tone and 2-tone excitations at five different current densities. Figs. 1 and 2 show MET model predictions for transducer gain, output power and drain efficiency versus available input power under one tone stimuli. Fig. 3 shows MET third order intermodulation distortion predictions versus peak envelope output power. Figs. 4 through 6 show the same results as above but with the isothermal Root model extracted at 25° C. Results show good accuracy between measured and modeled data for both models. Results also show better accuracy in the MET model as the device moves into gain compression, as well as better predictions of the transducer gain at multiple biases.

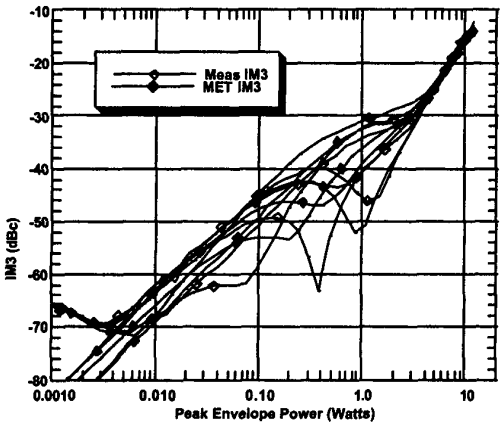

Fig. 3. Measured and simulated MET model IM3 vs. peak envelope power for a 10.2 mm LDMOS FET.

V. RFIC Design Environment

Designers were provided with an ADS design kit for our high voltage LDMOS IC process. This design kit includes electrical models and artwork generation routines for transmission lines, spiral inductors, resistors, and series and shunt capacitors elements as well as active devices. In addition, a model for the package was also developed, allowing the designer to completely simulate the electrical performance of the packaged circuit. With accurate simulation models as well as circuit layout capabilities, the design kit allows for a robust design environment.

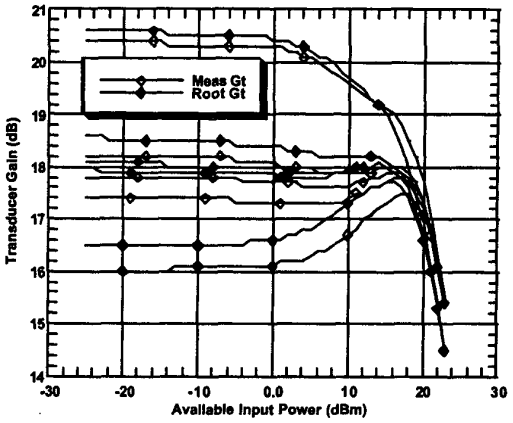

Fig. 4. Measured and simulated Root model transducer gain vs. available input power for a 10.2 mm LDMOS FET.

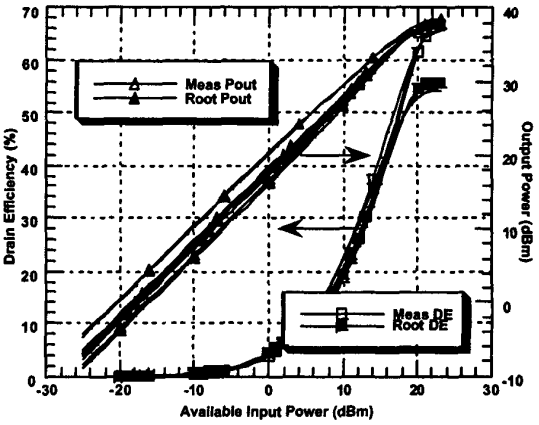

Fig. 5. Measured and simulated Root model drain efficiency and Pout vs. available input power for a 10.2 mm LDMOS FET.

The ADS only design flow provides several advantages over a hybrid or multi-tool design flow. For example, there is no need to duplicate schematic and layout libraries in more than one tool, which minimizes librarian activities within modeling groups. The biggest advantage of the one tool design flow is that it provides a unified design environment for RFIC circuit design, layout and design rule checking of ICs. Furthermore, the unified design environment also provides the ability to simulate the IC in a package and in a printed circuit board environment. Finally the availability of an electromagnetic simulator within the unified design environment, allows the designer to better simulate critical sections of the circuit at the IC

and/or the board level, increasing the chance for first pass design success.

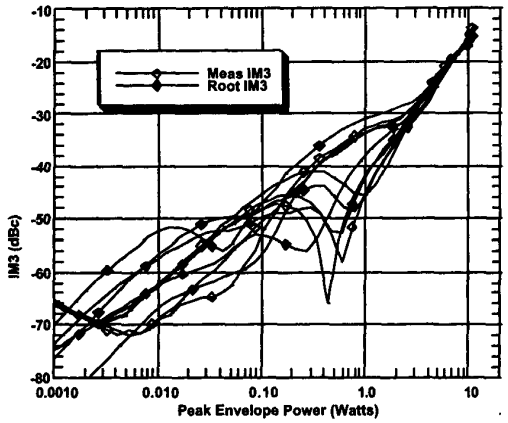

Fig. 6. Measured and simulated Root model IM3 vs. peak envelope power for a 10.2 mm LDMOS FET.

VI. RFIC PERFORMANCE

The high voltage Si LDMOS RF IC design kit has been used to successfully design several products. One example is a wide-band 30-Watt power amplifier in which the entire IC design was completed in ADS. As illustrated in Figs. 7 and 8, the RFIC design achieved 32 dB of Gain with 0.1 dB gain flatness over 50 MHz and -53 dBc IS-95 CDMA ACPR and 21% PAE (not shown) at 5 Watts average output power. This IC can also be used in multi-carrier applications.

VII. CONCLUSION

A robust model extraction procedure was successfully implemented for Motorola's high voltage Si LDMOS RFIC process. This modeling procedure yielded accurate large-signal transistor models that are used to achieve first pass linear RFIC amplifier designs. Also, all passive models needed for the design of the IC were developed and implemented into a design kit within Agilent's ADS to design a wide-band 30 Watt power amplifier IC which achieved first pass design success.

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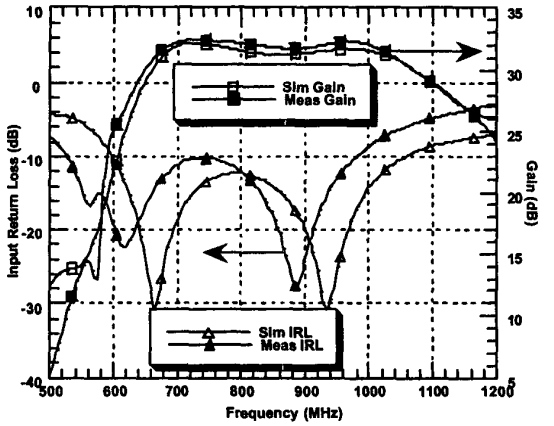

Fig. 7. Measured and simulated input return loss and gain vs. frequency of the 30 W power amplifier IC.

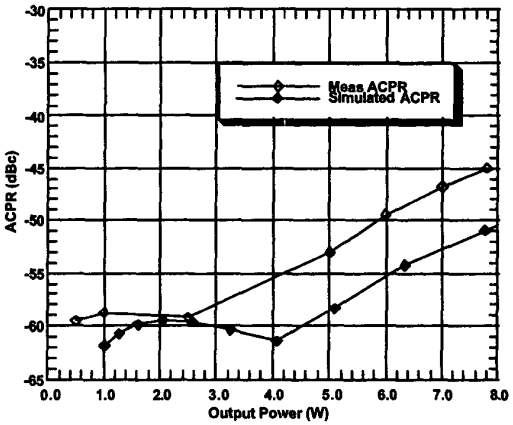

Fig. 8. Measured and simulated ACPR vs. average output power of the 30 W power amplifier IC.

REFERENCES

[1] J. Plá, "Characterization and modeling of high power RF semiconductor devices under constant and pulsed excitations", *Proceedings of the Fifth Annual Wireless Symposium*, pp. 467-472, February 1997.

[2] D.E. Root, S. Fan and J. Meyer, "Technology-independent large-signal FET models: a measurement-based approach to active device modeling", *Proc. 15th ARMMS Conference*, Bath, England, Paper #5, pp. 1-21, September 1991

[3] J. Plá & M. Purchine, "High power device modeling and characterization of high voltage Si LDMOS under constant and pulsed conditions", *HP-EEsof 1996 U.S. IC-CAP Users' Meeting Proceedings.*

[4] W.R. Curtice, J.A. Plá, D. Bridges, T. Liang, E.E. Shumate, "A new dynamic electro-thermal nonlinear model for silicon RF LDMOS FETs", *IEEE MTT-S IMS Digest*, Vol.2, pp. 419-422, 1999.